REMARKS

The outstanding Action been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

Claims 1-36 are pending in this application, of which claims 1 , 20-22, 35 and 36 are in independent form. By this Amendment, claims 35 and 36 have been amended to place the application in better condition for examination. No new matter has been added. As such, claims 1-36 are submitted for consideration.

Allowable Subject Matter

It is noted with appreciation that claims 8-16 and 23-34 have been indicated in item 8 of the outstanding Action as containing allowable subject matter, and that claim 20 has been indicated in item 9 of the outstanding Action as being allowed.

Section 112 Rejection

Claims 35 and 36 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

Claims 35 and 36 have been amended to address the Examiner's concerns as set forth in item 2 of the outstanding Action. Illustration thereof is shown in Fig. 13.

Section 102 Rejections

Claims 1-6, 18 and 35 have been rejected under 35 U.S.C. §102(b) as being anticipated by Collins et al. (U.S. Patent No. 6,031,847, hereinafter "*Collins*").

For the reasons set forth below, it is respectfully submitted that ***Collins*** does not disclose or teach each and every element of the present invention as set forth in independent claims 1-6, 18 and 35.

The present invention as set forth in claim 1 from which claims 2-6 and 18 directly or indirectly depend is not disclosed by ***Collins***. For instance, claim 1 requires that a logical value is expressed by an order, whereas in ***Collins***, the order in that the edges appear in signals in a word 501 simply does not express any logical value. More specifically, ***Collins*** discloses a dynamic skew compensation circuit for removing a signal skew due to a propagation delay in the signal line. Fig. 5 of ***Collins*** clearly illustrates that the edges of the signals in the word 501, expressing a logic of "1111" and transferred from a transmitter 301, are out of respective alignments due to skews (see also col. 8, lines 9-13 of ***Collins***).

Referring to the present application as set forth in claim 35, the outstanding Action asserts that the predetermined delay time recited therein corresponds to the skew in ***Collins***. However, a plurality of logical values cannot be expressed by the skew in ***Collins***. This is clear from the fact that, as mentioned above, the skew in ***Collins*** depends on a propagation delay of the signal line, and is constant in value.

Claim 21 is rejected under 35 U.S.C. §102(e) as being anticipated by Cecchi et al. (U.S. Patent No. 6,304,106, hereinafter "*Cecchi*").

For the reasons set forth below, it is respectfully submitted that ***Cecchi*** does not disclose or teach each and every element of the present invention as set forth in claim 21.

In ***Cecchi***, a logical value cannot be generated based on an order in timings that edges of the input signals appear, whereas the logical value as set forth in claim 21 can be generated based on such order. More specifically, ***Cecchi*** discloses a bi-directional communication link for transmitting/receiving data through a communication channel. In the link, a driver 102 generates current responsive to inputs A, B, and C, respectively, at output pins PAD and PADN (see Fig. 4 in ***Cecchi***), and a receiver 106 outputs a "1" or "0" (two values) according to the voltage difference between the output pins PAD and PADN (col. 3, lines 19-29 in ***Cecchi***).

Claims 1, 7, 22 and 36 are rejected under 35 U.S.C. §102(b) as being anticipated by *Jeong* (U.S. Patent No. 5,712,884).

For the reasons set forth below, it is respectfully submitted that ***Jeong*** does not disclose or teach each and every element of the present invention as set forth in claims 1, 7, 22 and 36.

In ***Jeong***, the logical values cannot be expressed by an order that edges of the parallel signals Q0-Q9 appear, whereas in the present invention as set forth in claim 1 from which claim 7 depends, the logical values can be expressed by such order. More specifically, ***Jeong*** discloses a data register 14 for converting/outputting a serial input signal DIL (input data) to parallel output signals Q0-Q9. As shown in Fig. 6 of ***Jeong***,

the output signals Q0-Q9 are always outputted in a predetermined order (e.g., Q0, Q1, Q2, ...).

Referring to claim 22, in ***Jeong***, the time difference between a transition edge of the output signal Q0 and a transition edge of the clock signal CK0 cannot be expressed by a plurality of logical values, whereas the time difference in the present invention as set forth in claim 22 can be expressed by such logical values. Moreover, in ***Jeong***, the output signals Q0-Q9 are outputted in synchronization with clock signals CK0-CK9, respectively (see Fig. 1 of ***Jeong***). The clock signals CK0-CK9 are outputted sequentially from delay cells 22 connected in series to each other. Therefore, the output signals Q0-Q9 are always outputted after internal delay time from the flip-flops 26, without depending on a logical value of the input signal DIL.

Referring to claim 36, the time difference between an edge of the output signal Q0 and an edge of the clock signal CK0 as disclosed in ***Jeong*** is the same when a logic level of the input signal DIL is "0" or "1", whereas in the present invention as set forth in claim 36, the time difference differs according to logic levels. This is evident from the fact that the logical value of output signals Q0-Q9 outputted from the flip-flops 26 does not depend on the delay time of delay cells 22, but rather it is dependent on a bit column of the serial input signal DIL.

Section 103 Rejection

Claim 19 is rejected under 35 U.S.C. §103(a) as being unpatentable over *Collins*.

In addition to the acknowledged deficiency in ***Collins*** relating to transmitter and receiver circuits, claim 19 is also distinguishable over ***Collins*** for at least the reasons stated above with respect to claim 1 since claim 19 depends from claim 1.

In view of the above remarks, the Applicant respectfully submits that each of claims 1-36 recites subject matter which is neither disclosed nor suggested in the cited prior art. Applicant therefore requests that each of claims 1-36 be found allowable, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account No. 01-2300.

Respectfully submitted,

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Enclosure: Marked-Up Copy of Amended Claims

MARKED-UP COPY OF AMENDED CLAIMS

35. (Amended) A semiconductor integrated circuit comprising:

a transmitting circuit for converting a logical value~~, expressed with a plurality of bits,~~ to a predetermined delay time in accordance with the logical value, the logical value being expressed with a plurality of bits, and for outputting a transmission signal, which is behind a standard timing signal by the delay time, to a signal line.

36. (Amended) A semiconductor integrated circuit comprising~~:~~ a receiving circuit for receiving a transmission signal, which is behind a standard timing signal by a predetermined delay time in accordance to a logical value,

for detecting a delay time ~~of~~ between a transition edge of ~~a~~ the transmission signal transmitting through a signal line, ~~to~~ and the transition edge of ~~a~~ the standard timing signal, and

for generating ~~a~~ the logical value according to the detected delay time.